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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,088	03/15/2004	Hiroyuki Shimada	9319S-000655	9497

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EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,088	SHIMADA, HIROYUKI	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/13/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Please verify the IDS filed on 3/15/2004.

U.S. document number 2002-001162 A1, date 1/31/2002 , name Hidea.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 5, 7 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Sekido et al. [JP- 05-075121] Applicant IDS.

With respect to claim 1, Sekido et al. (figs. 5-6, pages 5-7) discloses a semiconductor device comprising:

a semiconductor layer (11 or 51);

a source region (56S') formed in the semiconductor layer (51) (see fig. 6C);

a drain region (56D') formed in the semiconductor layer (51) (see fig. 6C);

a channel region (17 or 57) formed between the source region (56S') and the drain

region (56D') in the semiconductor layer (51) (see fig. 6C);

a gate insulating layer (14 or 54) formed above the channel region (17 or 57); and

a gate electrode (15 or 55) formed above the gate insulating layer (14 or 54), the gate electrode having a major axis and a minor axis;

wherein a boundary between the gate insulating layer (14 or 54) and the channel region (17 or 57) is a wave-like pattern of a gradual slope having crests and troughs alternately spaced apart along the major axis of the gate electrode (See fig. 5C).

With respect to claims 5 and 7, Sekido et al. discloses that a part of an upper surface of the source/drain region (56S'/56D') is flat (see fig. 6C).

With respect to claim 12, Sekido et al. (figs. 5-6, pages 5-7) discloses a semiconductor device comprising:

a semiconductor layer (11 or 51);

a source region (56S') formed in the semiconductor layer (51) (see fig. 6C);

a drain region (56D') formed in the semiconductor layer (51) (see fig. 6C);

a channel region (17 or 57) formed between the source region (56S') and the drain

region (56D') in the semiconductor layer (51) (see fig. 6C);

a gate insulating layer (14 or 54) formed above the channel region (17 or 57); and

a gate electrode (15 or 55) formed above the gate insulating layer (14 or 54), the gate electrode having a major axis and a minor axis;

wherein a boundary between the gate insulating layer (14 or 54) and the channel region (17 or 57) is a wave-like pattern of a gradual slope having crests and troughs alternately spaced apart along the major axis of the gate electrode (See fig. 5C).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4, 6, 8 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekido et al. [JP- 05-075121] Applicant IDS.

With respect to claims 2, 13 and 14, Sekido et al. (figs. 5-6, pages 5-7) discloses a semiconductor device comprising:

a semiconductor layer (11 or 51);

a source region (56S') formed in the semiconductor layer (51) (see fig. 6C);

a drain region (56D') formed in the semiconductor layer (51) (see fig. 6C);

a channel region (17 or 57) formed between the source region (56S') and the drain

region (56D') in the semiconductor layer (51) (see fig. 6C);

a gate insulating layer (14 or 54) formed above the channel region (17 or 57); and

a gate electrode (15 or 55) formed above the gate insulating layer (14 or 54), the gate electrode having a major axis and a minor axis;

wherein a boundary between the gate insulating layer (14 or 54) and the channel region (17 or 57) is a wave-like pattern (sinusoidal or curving), having crests and troughs alternately spaced apart along the major axis of the gate electrode (See fig. 5C).

Sekido et al. does not teach exactly the shape of the wave-like pattern as claimed by Applicant. However, the shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious.

With respect to claims 3-4, Sekido et al. discloses all the limitations as claimed above except a pitch between a top of the wave-like pattern and an adjacent bottom of the wave-like pattern in the boundary is less than or equal to 50 nm. However, the pitch range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant

must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claims 6 and 8, Sekido et al. discloses that a part of an upper surface of the source/drain region (56S'/56D') is flat (see fig. 6C).

5. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekido et al. [JP- 05-075121] Applicant IDS in view of Ker et al. [U.S. Pat. 6,750,515] previously applied.

Sekido et al. discloses all the limitations as claimed above except the semiconductor layer is formed above a support substrate with an insulating layer therebetween. However, Ker et al. discloses that the SOI substrate include the semiconductor layer (106) formed above a support substrate (100) with an insulating layer (102) therebetween (see fig. 3 and col. 4, lines 17-23). Therefore, it would have been obvious to one ordinary skill in the art to use SOI substrate as taught by Ker et al. into the device of Sekido et al. in order to prevent latch-up, junction capacitance and junction leakage current (see col. 1, lines 25-33).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAI PHAM
PRIMARY EXAMINER